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10/021,009	12/19/2001	Hong Sung Song	049128-5055	8778

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EXAMINER	
BODDIE, WILLIAM	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/021,009	SONG, HONG SUNG	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, March 22nd, 2007, the Applicant amended claims 1, 5, 10 and added new claims 21-23. Currently claims 1-15 and 21-23 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 22nd, 2007 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-15 and 21-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5-6, 10, 12-15 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Moon (US 5,825,343) and further in view of Mano et al. (US 6,072,451).

With respect to claim 1, Chen discloses, a method of driving a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of gate lines (G1-G4 in fig. 1a) in a matrix array, comprising the steps of:

supplying the data lines with (n-2)th data (D1 value at T3 in fig. 5) corresponding to the liquid crystal cells connected to an (n-2)th gate line (G1 in fig. 5), wherein n is an integer greater than 2;

conducting a first data supplying channel (note the selection pulse on G3 at T3 in fig. 5) for the liquid crystal cells connected to the nth gate line (G3 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the nth gate line;

conducting a second data supplying channel for the liquid crystal cells connected to the (n-2)th gate line (G1 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the (n-2)th gate line (note the voltage of pixel P11 in fig. 5),

wherein conducting the first data supplying channel and conducting the second data supplying channel are performed substantially simultaneously (both G1 and G3 are driven simultaneously at T3 in fig. 5; col. 3, lines 45-47).

Chen does not expressly disclose, supplying gate start pulses to conduct data supplying channels, or that the first and second gate start pulses are output from a pre-charging controller.

Moon discloses, supplying gate start pulses (note the two start pulses on STV in fig. 9) to a gate driver (2 in fig. 9), that in response generate pulses on gate electrodes

(col. 4, lines 59-63; for example), and that the first and second gate start pulses are output from a pre-charging controller (fig. 6; clear from fig. 6, that the device generates the STV signal pulses that are applied in fig. 9).

Chen and Moon are analogous art because they are both from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the gate start pulses, taught by Moon, to generate the gate electrode pulses of the LCD panel of Chen.

The motivation for doing so would have been to insure that an electric potential is sufficiently applied to the pixel, thereby causing correct gray level display and decreasing crosstalk (col. 2, lines 42-48; 29-33).

Neither Moon nor Chen expressly disclose that the pre-charging controller includes at least an exclusive OR gate.

Mano discloses, LCD drive circuitry to generate a select signal (fig. 47) that includes at least an exclusive OR gate (4703 in fig. 6; col. 28, line 48).

Mano, Chen and Moon are analogous art because they are all from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Moon and Chen with the XOR gates taught by Mano.

The motivation for doing so would have been to simplify the circuitry involved in generating the first and second gate start pulses.

With respect to claim 5, Chen discloses, a driving apparatus for a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of gate lines (G1-G4 in fig. 1a) in a matrix array comprising:

continuously generating first and second gate pulses (pulses on G3 and G1 for example, col. 4, lines 26-31) to supply an (n-2)th data corresponding to liquid crystal cells connected to an (n-2)th gate line to both liquid crystal cells connected to an nth gate line and liquid crystal cells connected to the (n-2)th gate line, wherein n is an integer greater than 2 (fig. 5; col. 3, lines 45-47).

Chen does not expressly disclose, a data/gate driving integrated circuit or a pre-charging controller that includes an XOR gate.

Moon discloses, a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel (col. 1, lines 52-59);

a gate driving integrated circuit (2 in fig. 9) responsive to first and second gate start pulses (two STV pulses in fig. 9) to sequentially drive the gate lines of the liquid crystal display panel (col. 4, lines 59-63); and

a pre-charging controller (fig. 6) to generate the first and second gate start pulses (clear from fig. 6, that the device generates the STV signal pulses that are applied in fig. 9).

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the driving apparatus', taught by Moon, in the LCD panel of Chen.

The motivation for doing so would have been to insure that a electric potential is sufficiently applied to the pixel, thereby causing correct gray level display and decreasing crosstalk (col. 2, lines 42-48; 29-33).

Neither Moon nor Chen expressly disclose that the pre-charging controller includes at least an exclusive OR gate.

Mano discloses, LCD drive circuitry to generate a select signal (fig. 47) that includes at least an exclusive OR gate (4703 in fig. 6; col. 28, line 48).

Mano, Chen and Moon are analogous art because they are all from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Moon and Chen with the XOR gates taught by Mano.

The motivation for doing so would have been to simplify the circuitry involved in generating the first and second gate start pulses.

With respect to claim 6, Chen and Moon disclose, the apparatus according to claim 5 (see above).

Moon further discloses, a counter and other logic circuits that generate pulses with timing seemingly identical to that of the Applicant's figures.

Neither Chen nor Moon expressly disclose the claimed inner circuitry of the pre-charging controller.

Mano discloses, LCD drive circuitry to generate select start signals (fig. 47) includes:

a first input line supplied with a pre-gate start pulse (Vsync; output of 4700 in fig. 47) and a second input line supplied with a data enable signal (looped input for 4701 and 4702 in fig. 47) for controlling data output of the data driving integrated circuit (col. 28, lines 37-64);

first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal (4701 in fig. 47);

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal (4702 in fig. 47); and

a gate device (4703 in fig. 47) for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay mean to continuously output the first and second gate start pulses (clear from fig. 47; also note col. 28, lines 37-64).

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Moon and Chen with the delay means and gates taught by Mano.

The motivation for doing so would have been to simplify the circuitry involved in generating the first and second gate start pulses.

With respect to claim 10, currently it appears that claim 10 is merely a broader version of claim 5, as it is exempt from the limitations of sequential gate driving and use of the dot inversion system. Therefore claim 10 is rejected based on the same merits shown above in the rejection of claim 5.

With respect to claim 12, Chen and Moon disclose, the method according to claim 10 (see above).

Chen further discloses, wherein polarity inversion of the data signals (D1 in fig. 5) applied to the liquid crystal cells connected to the first and second gate lines (G1, G2 in fig. 5) is made in at least two clock time intervals prior to an application of an active data signal (T3 for G1 and T4 for G2) (the pre-charge data must undergo polarity inversion prior to be applied (prior to T1 for G1), this is clearly two clock intervals prior to the application of active data (T3 for G1); also note col. 3, lines 39-45 and col. 4, lines 26-31).

With respect to claim 13, Chen and Moon disclose, the method according to claim 10 (see above).

Chen further discloses, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines (G1 and G2 in fig. 5) are applied in at least two clock time intervals before the gate and data control signals become effective data (fig. 5; Chen delays the control signals applied to the first and second gate lines; and also discloses different lengths of driving pulses; col. 3, lines 42-45; col. 4, lines 26-31).

With respect to claim 14, Moon and Chen disclose, the apparatus according to claim 10 (see above).

Chen further discloses, wherein the (n-2)th data is also supplied to liquid crystal cells connected to the (n-2)th gate line (clear from fig. 5, as well as col. 3, lines 45-47;

which discloses clearly that the same signal that is used for precharging in one time period for one gate line is another gate line's data signal).

With respect to claim 15, Moon, Mano and Chen disclose, the apparatus according to claim 10 (see above).

As the further limitations of claim 15 are identical limitations to claim 6, claim 15 is rejected on the same merits shown above in claim 6.

With respect to claims 21-23, Moon, Mano and Chen disclose, the apparatus according to claims 1, 5 and 10 (see above).

Neither Chen nor Moon expressly disclose the claimed inner circuitry of the pre-charging controller.

Mano further discloses, wherein the pre-charging gate controller further includes a first and second D flip-flop (4701 and 4702 in fig. 47).

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Moon and Chen with the D flip-flops taught by Mano.

The motivation for doing so would have been to simplify the circuitry involved in generating the first and second gate start pulses.

6. Claims 2-4, 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Moon (US 5,825,343) and Mano et al. (US 6,072,451) and further in view of Asada et al. (US 5,867,141).

With respect to claim 2, Chen, Mano and Moon disclose, the method according to claim 1 (see above).

Chen further discloses precharging the first and second gate lines at every frame with data signals (T1, T2 in fig. 5; col. 3, lines 39-45).

Neither Chen, Mano nor Moon expressly disclose that the first and second gate lines are precharged during a blanking interval.

Asada discloses precharging a first and second gate line with data signals applied during a blanking interval (abstract and col. 5, lines 18-38).

Chen, Mano, Moon and Asada are analogous art because they are both from the same field of endeavor namely, gate driving methods of liquid crystal displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to drive the LCD of Chen, Mano and Moon during T1-T2 as a blanking interval, as taught by Asada.

The motivation for doing so would have been to generate images with competent image quality and a stable high contrast (Asada; col. 3, lines 64-65).

With respect to claim 3, Chen, Mano, Moon and Asada disclose, the method according to claim 2 (see above).

Chen further discloses, wherein polarity inversion of the data signals (D1 in fig. 5) applied to the liquid crystal cells connected to the first and second gate lines (G1, G2 in fig. 5) is made in at least two clock time intervals prior to an application of an active data signal (T3 for G1 and T4 for G2) (the pre-charge data must undergo polarity inversion prior to be applied (prior to T1 for G1), this is clearly two clock intervals prior to the application of active data (T3 for G1); also note col. 3, lines 39-45 and col. 4, lines 26-31).

With respect to claim 4, Chen, Mano, Moon and Asada disclose, the method according to claim 2 (see above).

Chen further discloses, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines (G1 and G2 in fig. 5) are applied in at least two clock time intervals before the gate and data control signals become effective data (fig. 5; Chen delays the control signals applied to the first and second gate lines; and also discloses different lengths of driving pulses; col. 3, lines 42-45; col. 4, lines 26-31).

With respect to claim 7, Chen, Mano and Moon disclose, the apparatus according to claim 5 (see above).

Also shown above Asada discloses a blanking interval (see rejection of claim 2).

For further motivation and means of combining see the above rejection of claim 2.

With respect to claim 8-9, Chen, Mano, Moon and Asada disclose, the apparatus according to claim 7 (see above).

As claims 8-9 are identical limitations to those recited in claims 3-4 they are rejected on the same merits shown above.

With respect to claims 11, as claim 11 recites identical limitations as claim 7, claim 11 is rejected on the same merits shown above in the rejection of claim 7.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
6/7/07

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